

Hardware Generation for Performance

SPIRAL **Automating High Quality Software Production**

Tutorial at HPEC 2019

Franz Franchetti Tze Meng Low **Carnegie Mellon University**

Mike Franusich SpiralGen, Inc.







Tze Meng Low



Mike Franusich

Tutorial based on joint work with the Spiral team at CMU, UIUC, and Drexel



Software/Hardware Generation for Performance



Today's Computing Landscape

1 Gflop/s = one billion floating-point operations (additions or multiplications) per second





Intel Xeon 8180M 2.25 Tflop/s, 205 W 28 cores, 2.5—3.8 GHz 2-way—16-way AVX-512

IBM POWER9 768 Gflop/s, 300 W 24 cores, 4 GHz 4-way VSX-3



Nvidia Tesla V100 *7.8 Tflop/s, 300 W* 5120 cores, 1.2 GHz 32-way SIMT



Intel Xeon Phi 7290F *1.7 Tflop/s, 260 W* 72 cores, 1.5 GHz 8-way/16-way LRBni



Snapdragon 835 *15 Gflop/s, 2 W* 8 cores, 2.3 GHz A540 GPU, 682 DSP, NEON



Intel Atom C3858 *32 Gflop/s, 25 W* 16 cores, 2.0 GHz 2-way/4-way SSSE3



Dell PowerEdge R940 *3.2 Tflop/s, 6 TB, 850 W* 4x 24 cores, 2.1 GHz 4-way/8-way AVX



Summit 187.7 Pflop/s, 13 MW 9,216 x 22 cores POWER9 + 27,648 V100 GPUs

Software/Hardware Generation for Performance

Spiral

2019: What \$1M Can Buy You





Dell PowerEdge R940 *4.5 Tflop/s, 6 TB, 850 W* 4x 28 cores, 2.5 GHz



BittWare TeraBox 18M logic elements, 4.9 Tb/sec I/O 8 FPGA cards/16 FPGAs, 2 TB DDR4





AberSAN ZXP4 90x 12TB HDD, 1 kW 1PB raw



OSS FSAn-4 200 TB PCIe NVMe flash 80 GB/s throughput



Nvidia DGX-1 *8x Tesla V100, 3.2 kW* 170 Tflop/s, 128 GB





ISAs Longevity and Abstraction Power

F-16A/B, C/D, E/F, IN, IQ, N, V: Flying since 1974



Compare: Desktop/workstation class CPUs/machines

Assembly code compatible !!







x86 binary compatible, but 500x parallelism ?!

1972	1989	1994	2006	2011	2018
Intel 8008	IBM PC/XT compatible	IBM RS/6000-390	GeForce 8800	Xeon Phi	Xeon Platinum 8180M
0.2—0.8 MHz	8088 @ 8 MHz, 640kB RAM	256 MB RAM, 6GB HDD	1.3 GHz, 128 shaders	1.3 GHz, 60 cores	28 cores, 2.5-3.6 GHz
Intelligent terminal	360 kB FDD, 720x348 mono	67 MHz Power2+, AIX	16-way SIMT	8/16-way SIMD	2/4/8/16-way SIMD

10⁷ – 10⁸ compounded performance gain over 45 years



SpiralGen Algorithms and Mathematics: 2,500+ Years





Fast Fourier Transform





Carnegie Mellon



Programming/Languages Libraries Timeline

Popular performance programming languages

- 1953: Fortran
- **1973:** C
- 1985: C++
- 1997: OpenMP
- 2007: CUDA
- 2009: OpenCL

Popular performance libraries

- 1979: BLAS
- 1992: LAPACK
- 1994: MPI
- 1995: ScaLAPACK
- 1995: PETSc
- 1997: FFTW

Popular productivity/scripting languages

- 1987: Perl
- **1989:** Python
- 1993: Ruby
- 1995: Java
- **2000:** C#





The Problem: Example DFT



- Standard desktop computer, cutting edge compiler, using optimization flags
- Implementations have same operations count: ≈4nlog₂(n)
- **Same plots can be shown for all mathematical functions**

DFT Plot: Analysis

nira

ftware/Hardware Generation for Performance

DFT (single precision) on Intel Core i7 (4 cores, 2.66 GHz) Performance [Gflop/s]



High performance library development has become a nightmare





How The Generated Code Looks Like

```
void dft64(float *Y, float *X) {
     m512 U912, U913, U914, U915, U916, U917, U918, U919, U920, U921, U922, U923, U924, U925,...;
   a2153 = ((m512 *) X); s1107 = *(a2153);
    s1108 = *((a2153 + 4)); t1323 = mm512 add ps(s1107, s1108);
   U926 = mm512 swizupconv r32( mm512 set 1to16 ps(0.70710678118654757), MM SWIZ REG CDAB);
    s1121 = mm512 madd231 ps( mm512 mul ps( mm512 mask or pi(
        mm512 set 1to16 ps(0.70710678118654757), 0xAAAA,a2154,U926),t1341),
        mm512 mask sub ps( mm512 set 1to16 ps(0.70710678118654757),0x5555,a2154,U926),
        mm512 swizupconv r32(t1341, MM SWIZ REG CDAB));
   U927 = mm512 swizupconv r32( mm512 set 16to16 ps(0.70710678118654757, (-0.70710678118654757),
        0.70710678118654757, (-0.70710678118654757), 0.70710678118654757, (-0.70710678118654757),
        0.70710678118654757, (-0.70710678118654757), 0.70710678118654757, (-0.70710678118654757),
        0.70710678118654757, (-0.70710678118654757), 0.70710678118654757, (-0.70710678118654757),
        0.70710678118654757, (-0.70710678118654757)), MM SWIZ REG CDAB);
    s1166 = mm512 madd231 ps( mm512 mul ps( mm512 mask or pi( mm512 set 16to16 ps(
        0.70710678118654757, (-0.70710678118654757), 0.70710678118654757, (-0.70710678118654757),
        0.70710678118654757, (-0.70710678118654757), 0.70710678118654757, (-0.70710678118654757),
        0.70710678118654757, (-0.70710678118654757), 0.70710678118654757, (-0.70710678118654757),
        0.70710678118654757, (-0.70710678118654757), 0.70710678118654757, (-0.70710678118654757)),
        0xAAAA,a2154,U951),t1362),
        mm512 mask sub ps( mm512 set 16to16 ps(0.70710678118654757,
        (-0.70710678118654757), 0.70710678118654757, (-0.70710678118654757), 0.70710678118654757,
        (-0.70710678118654757), 0.70710678118654757, (-0.70710678118654757), 0.70710678118654757,
        (-0.70710678118654757), 0.70710678118654757, (-0.70710678118654757), 0.70710678118654757,
        (-0.70710678118654757), 0.70710678118654757, (-0.70710678118654757)), 0x5555, a2154, U951),
        mm512 swizupconv r32(t1362, MM SWIZ REG CDAB));
}
```

D. McFarlin, F. Franchetti, and M. Püschel: Automatic Generation of Vectorized Fast Fourier Transform Libraries for the Larrabee and AVX Instruction Set Extension. Proceedings of the 2009 High Performance Embedded Computing (HPEC), MIT Lincoln Laboratory. Best paper award.

Software/Hardware Generation for Performance



Goal: Go from Mathematics to Software

Given:

 Mathematical problem specification does not change

Computer platform

changes often

Wanted:

- Very good implementation of specification on platform
- Proof of correctness





The Spiral System

Traditionally



Spiral Approach



Vision Behind Spiral

Current





- C code a singularity: Compiler has no access to high level information
- Challenge: conquer the high abstraction level for complete automation





How Spiral Works

Problem specification ("DFT 1024" or "DFT")

Complete automation of

the implementation and optimization task

Basic ideas:

- **Declarative representation** of algorithms
- Rewriting systems to generate and optimize algorithms at a high level of abstraction







Spiral's Domain-Specific Program Synthesis

Model: common abstraction = spaces of matching formulas



Spiral<mark>Gen</mark>

Software/Hardware Generation for Performance

Inspiration: Symbolic Integration

- Rule based AI system basic functions, substitution
- May not succeed not all expressions can be symbolically integrated
- Arbitrarily extensible

define new functions as integrals Γ(.), distributions, Lebesgue integral

Semantics preserving rule chain = formal proof

Automation

Mathematica, Maple

Table of Integrals

BASIC FORMS

- $(1) \qquad \int x^n dx = \frac{1}{n+1} x^{n+1}$
- (2) $\int \frac{1}{x} dx = \ln x$
- (3) $\int u dv = uv \int v du$
- $(4) \qquad \int u(x)v'(x)dx = u(x)v(x) \int v(x)u'(x)dx$

RATIONAL FUNCTIONS

- (5) $\int \frac{1}{ax+b} dx = \frac{1}{a} \ln(ax+b)$
- (6) $\int \frac{1}{(x+a)^2} dx = \frac{-1}{x+a}$
- (7) $\int (x+a)^n dx = (x+a)^n \left(\frac{a}{1+n} + \frac{x}{1+n}\right), \ n \neq -1$
- (8) $\int x(x+a)^n dx = \frac{(x+a)^{1+n}(nx+x-a)}{(n+2)(n+1)}$









Out[33]= 0





Example 1: SAR for Cell BE



Result

Same performance, 1/10th human effort, non-expert user

Key ideas

restrict domain, use mathematics, performance portability

D. McFarlin, F. Franchetti, M. Püschel, and J. M. F. Moura: **High Performance Synthetic Aperture Radar Image Formation On Commodity Multicore Architectures.** in Proceedings SPIE, 2009. ftware/Hardware Generation for Performance

Carnegie Mellon



Example 2: Density Functional Theory



3.5 GHz, AVX, double precision, interleaved input, single core

Performance [Pseudo Gflop/s]



Input data cube edge length

Unusual requirements:

- Odd FFT sizes
- Small sizes
- Rectangular box



P. D. Haynes, C.-K. Skylaris, A. A. Mostofi and M. C. Payne, "ONETEP: linear-scaling density-functional theory with plane waves," Psi-k Newsletter 72, 78-91 (December 2005)

T. Popovici, F. Russell, K. Wilkinson, C-K. Skylaris, P. H. J. Kelly, F. Franchetti, "Generating Optimized Fourier Interpolation Routines for Density Functional Theory Using SPIRAL," 29th International Parallel & Distributed Processing Symposium (IPDPS), 2015.







guantum-mechanical calculations based on density-functional theory

Core operation: FFT-based 3D 2x2x2 upsampling



Software/Hardware Generation for Performance Example 3: Synthesis of Production Code

s3013 = _mm_loadl_pi(a772, ((float *) X)); s3014 = _mm_loadl_pi(a772, ((float *) (X ± 2))) ((float *) (X ± 6)));

Spiral-Synthesized code in Intel's Library IPP 6 and 7

- IPP = Intel's performance primitives, part of Intel C++ Compiler suite
- Generated: 3984 C functions (signal processing) = 1M lines of code
- Full parallelism support
- Computer-generated code: Faster than what was achievable by hand

```
s3017 = mm loadl pi(a772, ((float *) (X + 14)));
s3018 = mm loadh pi(mm loadl pi(a772, ((float *) (X + 24))), ((float *) (X + 20)));
s3019 = mm loadl pi(a772, ((float *) (X + 8)));
s3020 = mm loadh pi(mm loadl pi(a772, ((float *) (X + 10))), ((float *) (X + 4)));
s3021 = mm loadl pi(a772, ((float *) (X + 12)));
s3022 = mm shuffle ps(s3014, s3015, MM SHUFFLE(2, 0, 2, 0));
s3023 = mm shuffle_ps(s3014, s3015, _MM_SHUFFLE(3, 1, 3, 1));
s3024 = _mm_shuffle_ps(s3016, s3017, _MM_SHUFFLE(2, 0, 2, 0));
                                                                                                 Intel<sup>®</sup>
s3025 = mm shuffle ps(s3016, s3017, MM SHUFFLE(3, 1, 3, 1));
s3026 = mm shuffle ps(s3018, s3019, MM SHUFFLE(2, 0, 2, 0));
                                                                                                 Integrated
s3027 = mm shuffle ps(s3018, s3019, MM SHUFFLE(3, 1, 3, 1));
                                                                                                 Performance
s3028 = mm shuffle ps(s3020, s3021, MM SHUFFLE(2, 0, 2, 0));
s3029 = mm shuffle ps(s3020, s3021, MM SHUFFLE(3, 1, 3, 1));
                                                                                                 Primitives
t3794 = mm add ps(s3042, s3043);
t3795 = mm add ps(s3038, t3793);
t3796 = mm add ps(s3041, t3794);
t3797 = mm sub ps(s3038, mm mul ps( mm set1 ps(0.5), t3793));
t3798 = mm sub ps(s3041, mm mul ps( mm set1 ps(0.5), t3794));
s3044 = mm mul ps( mm set1 ps(0.8660254037844386), mm sub ps(s3042, s3043));
s3045 = mm mul ps( mm set1 ps(0.8660254037844386), mm sub ps(s3039, s3040));
t3799 = mm add ps(t3797, s3044);
t3800 = mm sub ps(t3798, s3045);
t3801 = mm sub ps(t3797, s3044);
t3802 = mm add ps(t3798, s3045);
a773 = mm mul ps( mm set ps(0, 0, 0, 1), mm shuffle ps(s3013, a772, MM SHUFFLE(2, 0, 2, 0)));
t3803 = mm add ps(a773, mm mul ps( mm set ps(0, 0, 0, 1), t3795));
a774 = mm mul ps( mm set ps(0, 0, 0, 1), mm shuffle ps(s3013, a772, MM SHUFFLE(3, 1, 3, 1)));
t_{3804} = mm add ps(a774, mm mul ps(mm set ps(0, 0, 0, 1), t_{3796}));
t3805 = mm add ps(a773, mm add ps( mm mul ps( mm set ps(0.28757036473700154, 0.30046260628866578, (-0.28757036473700154), (-0.083333333333333333
t3806 = mm add ps(a774, mm add ps( mm mul ps( mm set ps(0.08706930057606789, 0, 0.087069300576068001, 0), t3795), mm mul ps( mm set ps(0.287
s3046 = mm sub ps( mm mul ps( mm set ps((-0.25624767158293649), 0.25826039031174486, (-0.30023863596633249), 0.075902986037193879), t3799), mm
s_{3047} = mm_{2}dd_{pg}/mm_{mul} pg/mm_{got} pg/(0.15680130105158462) (-0.15355568557054136) (-0.011500105605768103) (0.20071724147084000) +3700)
```



Carnegie Mellon

Software/Hardware Generation for Performance

Selected Results: FFTs and Spectral Algorithms



Performance of 2x2x2 Upsampling on Haswell

3.5 GHz, AVX, double precision, interleaved input, single core

Performance [Pseudo Gflop/s]





BlueGene/P at Argonne National Laboratory 128k cores (quad-core CPUs) at 850 MHz

PFA SAR Image Formation on Intel platforms

performance [Gflop/s]







Current Work: FFTX and SpectralPACK



Spectral Algorithms



Define the LAPACK equivalent for spectral algorithms

- Define FFTX as the BLAS equivalent provide user FFT functionality as well as algorithm building blocks
- Define class of numerical algorithms to be supported by SpectralPACK
 PDE solver classes (Green's function, sparse in normal/k space,...), signal processing,...
- Library front-end, code generation and vendor library back-end mirror concepts from FFTX layer

Spiral provides backend code generation and autotuning



SpiralGen

SPIRAL 8.1.0: Open Source

Open Source SPIRAL available

- non-viral license (BSD)
- Initial version, effort ongoing to open source whole system
- Open sourced under DARPA PERFECT
- Commercial support via SpiralGen, Inc.

Developed over 20 years Funding: DARPA (OPAL, DESA, HACMS, PERFECT, BRASS), NSF, ONR, DoD HPC, JPL,

DOE, CMU SEI, Intel, Nvidia, Mercury





www.spiral.net

s14 = (a49 + a50);

F. Franchetti, T. M. Low, D. T. Popovici, R. M. Veras, D. G. Spampinato, J. R. Johnson, M. Püschel, J. C. Hoe, J. M. F. Moura: **SPIRAL: Extreme Performance Portability,** Proceedings of the IEEE, Vol. 106, No. 11, 2018. Special Issue on *From High Level Specification to High Performance Code*



Organization

re/Hardware Generation for Perfo

- SPL: Problem and algorithm specification
- **Σ-SPL:** Automating high level optimization
- Rewriting: Formal parallelization
- Rewriting: Vectorization
- Verification
- Spiral as FFTX backend
- Summary

F. Franchetti, T. M. Low, D. T. Popovici, R. M. Veras, D. G. Spampinato, J. R. Johnson, M. Püschel, J. C. Hoe, J. M. F. Moura: **SPIRAL: Extreme Performance Portability,** Proceedings of the IEEE, Vol. 106, No. 11, 2018. Special Issue on *From High Level Specification to High Performance Code*





What is a (Linear) Transform?

Mathematically: Matrix-vector multiplication

$$\begin{array}{ccc} x\mapsto y=T\cdot x\\ \text{input vector (signal)} & \begin{array}{c} & & \\ & & \\ \end{array} \end{array} \begin{array}{c} & & \\ & & \\ \end{array} \end{array} \begin{array}{c} & & \\ & & \\ \end{array} \begin{array}{c} & & \\ & & \\ \end{array} \end{array} \begin{array}{c} & & \\ & & \\ \end{array} \begin{array}{c} & & \\ & & \\ \end{array} \begin{array}{c} & & \\ & & \\ \end{array} \end{array} \begin{array}{c} & & \\ & & \\ \end{array} \begin{array}{c} & & \\ & & \\ \end{array} \begin{array}{c} & & \\ & & \\ \end{array} \end{array} \begin{array}{c} & & \\ & & \\ \end{array} \end{array}$$

Example: Discrete Fourier transform (DFT)

$$\mathbf{DFT}_n = [e^{-2k\ell\pi i/n}]_{0 \le k, \ell < n}$$



Transform Algorithms: Example 4-point FFT

Cooley/Tukey fast Fourier transform (FFT):

$$\begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & j & -1 & -j \\ 1 & -1 & 1 & -1 \\ 1 & -j & -1 & j \end{bmatrix} = \begin{bmatrix} 1 & \cdot & 1 & \cdot \\ \cdot & 1 & \cdot & 1 \\ \cdot & 1 & -1 & \cdot \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & 1 & \cdot & \cdot \\ 1 & -1 & \cdot & \cdot \\ \cdot & 1 & 1 & \cdot \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & \cdot & \cdot \\ \cdot & 1 & \cdot & \cdot \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & \cdot & \cdot \\ \cdot & 1 & \cdot & \cdot \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & \cdot & \cdot \\ \cdot & 1 & \cdot & \cdot \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & \cdot & \cdot \\ \cdot & 1 & \cdot & \cdot \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & \cdot & \cdot \\ \cdot & 1 & \cdot & \cdot \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & \cdot & \cdot \\ \cdot & 1 & \cdot & \cdot \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & \cdot & \cdot \\ \cdot & 1 & \cdot & \cdot \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & \cdot & \cdot \\ \cdot & 1 & \cdot & \cdot \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & \cdot & \cdot \\ \cdot & 1 & \cdot & \cdot \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & \cdot & \cdot \\ \cdot & 1 & \cdot & \cdot \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & \cdot & \cdot \\ \cdot & 1 & \cdot & \cdot \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & \cdot & \cdot \\ \cdot & 1 & \cdot & \cdot \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & \cdot & \cdot \\ \cdot & 1 & \cdot & \cdot \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & \cdot & \cdot \\ \cdot & 1 & \cdot & \cdot \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & \cdot & \cdot \\ \cdot & 1 & \cdot & \cdot \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & \cdot & \cdot \\ \cdot & 1 & \cdot & \cdot \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & \cdot & \cdot \\ \cdot & 1 & -1 & \cdot \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & \cdot & \cdot \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & \cdot & \cdot \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & \cdot & \cdot \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & \cdot & \cdot \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & \cdot & \cdot \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & \cdot & \cdot \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & \cdot & 1 \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & \cdot & 1 \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & \cdot & 1 \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & \cdot & 1 \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & \cdot & 1 \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & \cdot & 1 \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & \cdot & 1 \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & \cdot & 1 \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & \cdot & 1 \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & \cdot & 1 \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & 1 & \cdot & 1 \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & 1 & -1 \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & 1 & -1 \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & 1 & -1 \\ \cdot & \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & 1 & -1 \\ \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & 1 & -1 \\ \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & \cdot & 1 & -1 \\ \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & 1 & -1 & -1 \\ \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & 1 & -1 & -1 \\ \cdot & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & 1 & -1 & -1 \end{bmatrix} \begin{bmatrix} 1 & 1 & -1 & -1 \\ \cdot & 1$$

Kronecker product Identity

Permutation

- Algorithms are divide-and-conquer: Breakdown rules
- Mathematical, declarative representation: SPL (signal processing language)
- SPL describes the structure of the dataflow







Examples: Transforms

$$\begin{aligned} \mathbf{D}\mathbf{C}\mathbf{T}\mathbf{-2}_{n} &= \left[\cos(k(2\ell+1)\pi/2n)\right]_{0\leq k,\ell < n},\\ \mathbf{D}\mathbf{C}\mathbf{T}\mathbf{-3}_{n} &= \mathbf{D}\mathbf{C}\mathbf{T}\mathbf{-2}_{n}^{T} \quad (\text{transpose}),\\ \mathbf{D}\mathbf{C}\mathbf{T}\mathbf{-4}_{n} &= \left[\cos((2k+1)(2\ell+1)\pi/4n)\right]_{0\leq k,\ell < n},\\ \mathbf{I}\mathbf{M}\mathbf{D}\mathbf{C}\mathbf{T}_{n} &= \left[\cos((2k+1)(2\ell+1+n)\pi/4n)\right]_{0\leq k<2n,0\leq \ell < n},\\ \mathbf{R}\mathbf{D}\mathbf{F}\mathbf{T}_{n} &= \left[r_{k\ell}\right]_{0\leq k,\ell < n}, \quad r_{k\ell} = \begin{cases} \cos\frac{2\pi k\ell}{n}, \quad k\leq \lfloor\frac{n}{2}\rfloor\\ -\sin\frac{2\pi k\ell}{n}, \quad k> \lfloor\frac{n}{2}\rfloor,\\ -\sin\frac{2\pi k\ell}{n}, \quad k> \lfloor\frac{n}{2}\rfloor,\\ \mathbf{W}\mathbf{H}\mathbf{T}_{n/2} \quad \mathbf{W}\mathbf{H}\mathbf{T}_{n/2}\\ \mathbf{W}\mathbf{H}\mathbf{T}_{n/2} - \mathbf{W}\mathbf{H}\mathbf{T}_{n/2}\\ \mathbf{M}\mathbf{H}\mathbf{T}_{n/2} \end{bmatrix}, \quad \mathbf{W}\mathbf{H}\mathbf{T}_{2} = \mathbf{D}\mathbf{F}\mathbf{T}_{2},\\ \mathbf{D}\mathbf{H}\mathbf{T} &= \left[\cos(2k\ell\pi/n) + \sin(2k\ell\pi/n)\right]_{0\leq k,\ell < n}.\end{aligned}$$







Examples: Breakdown Rules (currently ≈220)

Combining these rules yields many algorithms for every given transform

Software/Hardware Generation for Performance





Breakdown Rules (>200 for >50 Transforms)

• "Teaches" Spiral algorithm knowledge

• Combining these rules yields many algorithms for every given transform

Software/Hardware Generation for Performance

Carnegie Mellon



Example FFT: Iterative FFT Algorithm $DFT_{r^{k}} = \left(\prod_{i=0}^{k-1} (I_{r^{i}} \otimes DFT_{r} \otimes I_{r^{k-i-1}}) D_{i}^{r^{k}}\right) R_{r}^{r^{k}}$



 $\left((I_1 \otimes \mathrm{DFT}_2 \otimes I_8) D_0^{16}\right) \left((I_2 \otimes \mathrm{DFT}_2 \otimes I_4) D_1^{16}\right) \left((I_4 \otimes \mathrm{DFT}_2 \otimes I_2) D_2^{16}\right) \left((I_8 \otimes \mathrm{DFT}_2 \otimes I_1) D_3^{16}\right) R_2^{16}$





Example FFT: Recursive FFT Algorithm

 $\mathrm{DFT}_{km} \stackrel{\bullet}{=} (\mathrm{DFT}_k \otimes I_m) T_m^n (I_k \otimes \mathrm{DFT}_m) L_k^n$



 $(\mathrm{DFT}_2 \otimes I_8)T_8^{16} \Big(I_2 \otimes \Big((\mathrm{DFT}_2 \otimes I_4)T_4^8 \big(I_2 \otimes \big((\mathrm{DFT}_2 \otimes I_2)T_2^4 (I_2 \otimes \mathrm{DFT}_2)L_2^4 \big) \big) L_2^8 \Big) \Big) L_2^{16}$



SPL Compiler

SPL construct	code		
$y = (A_n B_n) x$	t[0:1:n-1] = B(x[0:1:n-1]); y[0:1:n-1] = A(t[0:1:n-1];)		
$y = (I_m \otimes A_n)x$	<pre>for (i=0;i<m;i++) y[i*n:1:i*n+n-1]="A(x[i*n:1:i*n+n-1])</pre"></m;i++)></pre>		
$y = (A_m \otimes I_n)x$	<pre>for (i=0;i<m;i++) y[i:n:i+m-1]="A(x[i:n:i+m-1]);</pre"></m;i++)></pre>		
$y = \left(\bigoplus_{i=0}^{m-1} A_n^i\right) x$	<pre>for (i=0;i<m;i++) y[i*n:1:i*n+n-1]="</td"></m;i++)></pre>		
$y = D_{m,n}x$	<pre>for (i=0;i<m*n;i++) y[i]="Dmn[i]*x[i];</pre"></m*n;i++)></pre>		
$y = L_m^{mn} x$	<pre>for (i=0;i<m;i++) (j="0;j<n;j++)" for="" y[i+m*j]="x[n*i+j];</pre"></m;i++)></pre>		

Example: tensor product

$$\mathbf{I}_m \otimes A_n = \begin{bmatrix} A_n & & \\ & \ddots & \\ & & A_n \end{bmatrix}$$

Works well for basic blocks. Loops and parallelization: next



Organization

are/Hardware Generation for Perfo

- SPL: Problem and algorithm specification
- **Σ-SPL:** Automating high level optimization
- Rewriting: Formal parallelization
- Rewriting: Vectorization
- Verification
- Spiral as FFTX backend
- Summary

F. Franchetti, Y. Voronenko, M. Püschel: Loop Merging for Signal Transforms Proceedings Programming Language Design and Implementation (PLDI) 2005, pages 315-326.



Spiral<mark>Gen</mark>

Problem: Fusing Permutations and Loops

🕏 Spiral







Software/Hardware Generation for Performance



New Approach for Loop Merging



Σ-SPL

tware/Hardware Generation for Performance

- Four central constructs: S, G, S, Perm
 - Σ (sum) makes loops explicit
 - G_f (gather) reads data using the index mapping f
 - $S_f(\text{scatter})$ writes data using the index mapping f
 - $Perm_f$ permutes data using the index mapping f
 - Every Σ-SPL formula still represents a matrix factorization



Software/Hardware Generation for Performance



Loop Merging With Rewriting Rules







Application: Loop Merging For FFTs

DFT breakdown rules:

Cooley-Tukey FFT
$$DFT_{km} \rightarrow (DFT_k \otimes I_m) T_m^{km} (I_k \otimes DFT_m) L_k^{km}$$

Prime factor FFT $DFT_{km} \rightarrow (V_{k,m}^T) DFT_k \otimes I_m) (I_k \otimes DFT_m) (V_{k,m})$
 $gcd(k,m) = 1$
Rader FFT $DFT_p \rightarrow (V_p^T) I_1 \oplus DFT_{p-1}) D_p (I_1 \oplus DFT_{p-1}) (V_p)$

Index mapping functions are **non-trivial**:

$$\begin{array}{lll} \mathsf{L}_{k}^{km} & \to & \mathsf{Perm}_{\ell_{k}^{km}} & & \ell_{k}^{km}(i) \ = \ \left\lfloor \frac{i}{m} \right\rfloor + k(i \mod m) \\ \mathsf{V}_{k,m} & \to & \mathsf{Perm}_{v_{k,m}} & & v_{k,m}(i) \ = \left(m \left\lfloor \frac{i}{m} \right\rfloor + k(i \mod m) \right) \mod km \\ \mathsf{W}_{p} & \to & \mathsf{Perm}_{w_{1,g}^{p}} & & w_{\phi,g}^{p}(i) \ = \ \begin{cases} \mathsf{0}, & i = \mathsf{0}, \\ \phi g^{i} \mod p, & \mathsf{else.} \end{cases} \end{cases}$$






Task: Index simplification





Index Simplification: Basic Idea

Example: Identity necessary for fusing successive

Rader and prime-factor step

$$\left(arphi g^{(b+si) \mod N'}
ight) \mod N = \left((arphi g^b) (g^s)^i
ight) \mod N$$

 $s |N', N'|N, \ 0 \le i < n$

Performed at the Σ -SPL level through rewrite rules on function objects:

$$\overline{w}_{\phi,g}^{N' \to N} \circ \overline{h}_{b,s}^{n \to N'} \to \overline{w}_{\phi g^b,g^s}^{n \to N}$$

Advantages: no analysis necessary efficient (or doable at all) Software/Hardware Generation for Performance

```
// Input: Complex double x[28], output: y[28]
double t1[28];
for(int i5 = 0; i5 <= 27; i5++)
    t1[i5] = x[(7*3*(i5/7) + 4*2*(i5%7))%28];
for(int i1 = 0; i1 <= 3; i1++) {
    double t3[7], t4[7], t5[7];
    for(int i6 = 0; i6 \le 6; i6++)
        t5[i6] = t1[7*i1 + i6];
    for(int i8 = 0; i8 \le 6; i8++)
        t4[i8] = t5[i8 ? (5*pow(3, i8))%7 : 0];
    {
        double t7[1], t8[1];
        t8[0] = t4[0];
        t7[0] = t8[0];
        t3[0] = t7[0];
        double t10[6], t11[6], t12[6];
        for(int i13 = 0; i13 <= 5; i13++)</pre>
            t12[i13] = t4[i13 + 1];
        for(int i14 = 0; i14 <= 5; i14++)
            t11[i14] = t12[(i14/2) + 3*(i1482)];
        for(int i3 = 0; i3 \le 2; i3++) {
            double t14[2], t15[2];
            for(int i15 = 0; i15 <= 1; i15++)</pre>
                t15[i15] = t11[2*i3 + i15];
            t14[0] = (t15[0] + t15[1]);
            t14[1] = (t15[0] - t15[1]);
            for(int i17 = 0; i17 <= 1; i17++)
                 t10[2*i3 + i17] = t14[i17];
        for(int i19 = 0; i19 <= 5; i19++)</pre>
            t3[i19 + 1] = t10[i19];
    for(int i20 = 0; i20 <= 6; i20++)
        y[7*i1 + i20] = t3[i20];
```

After, 2 Loops

Before, 11 Loops



Organization

- SPL: Problem and algorithm specification
- **Σ-SPL:** Automating high level optimization
- Rewriting: Formal parallelization
- Rewriting: Vectorization
- Verification
- Spiral as FFTX backend
- Summary

F. Franchetti, Y. Voronenko, S. Chellappa, J. M. F. Moura, and M. Püschel
Discrete Fourier Transform on Multicores: Algorithms and Automatic Implementation
IEEE Signal Processing Magazine, special issue on "Signal Processing on Platforms with Multiple Cores", 2009.



One Approach for All Types of Parallelism

- Shared Memory (Multicore)
- Vector SIMD (SSE, VMX, Double FPU...)
- Message Passing (Clusters)
- Graphics Processors (GPUs)
- FPGA

vare/Hardware Generation for Performance

- HW/SW partitioning
- Multiple Levels of Parallelism (Cell BE)





optimized/adapted implementation







SPL to Shared Memory Code: Basic Idea

Good construct: tensor product

$$y = (\mathbf{I}_p \otimes A) x$$



p-way embarrassingly parallel, load-balanced

Problematic construct: permutations produce false sharing



Task: Rewrite formulas to extract tensor product + treat cache lines as atomic







Step 1: Shared Memory Tags

Identify crucial hardware parameters

- Number of processors: p
- Cache line size: μ
- Introduce them as tags in SPL:



This means: formula A is to be optimized for p processors and cache line size μ

Tags express hardware constraints within the rewriting system





Step 2: Identify "Good" Formulas

Load balanced, avoiding false sharing

 $y = \left(\mathbf{I}_p \otimes A\right) x \quad \text{with} \quad A \in \mathbb{C}^{m\mu \times m\mu}$ $y = \left(\bigoplus_{i=0}^{p-1} A_i\right) x \quad \text{with} \quad A_i \in \mathbb{C}^{m\mu \times m\mu}$ $y = \left(P \otimes \mathbf{I}_\mu\right) x \quad \text{with} \ P \text{ a permutation matrix}$

Tagged operators (no further rewriting necessary)

$$\mathbf{I}_p \otimes_{\parallel} A, \quad \bigoplus_{i=0}^{p-1} ||A_i, \quad P \overline{\otimes} \mathbf{I}_{\mu}|$$

Definition: A formula is fully optimized if it is one of the above or of the form

$$\mathbf{I}_m \otimes A$$
 or AB

where A and B are fully optimized.





Step 3: Identify Rewriting Rules

Goal: Transform formulas into fully optimized formulas

- Formulas rewritten, tags propagated
- There may be choices

$$\begin{split} \underbrace{AB}_{\text{smp}(p,\mu)} &\to \underbrace{A}_{\text{smp}(p,\mu)} \underbrace{B}_{\text{smp}(p,\mu)} \\ \underbrace{Am \otimes I_n}_{\text{smp}(p,\mu)} &\to \underbrace{\left(\bigsqcup_{m}^{mp} \otimes I_{n/p} \right) \left(I_p \otimes (A_m \otimes I_{n/p}) \right) \left(\bigsqcup_{p}^{mp} \otimes I_{n/p} \right)}_{\text{smp}(p,\mu)} \\ \underbrace{\bigcup_{m}^{mn}}_{\text{smp}(p,\mu)} &\to \underbrace{\left\{ \underbrace{\left(I_p \otimes \bigsqcup_{m/p}^{mn/p} \right) \left(\bigsqcup_{p}^{pn} \otimes I_{m/p} \right)}_{\text{smp}(p,\mu)} \left(\underbrace{\bigsqcup_{p}^{pm} \otimes I_{n/p} \right) \left(\underbrace{\bigsqcup_{p}^{pm} \otimes I_{n/p} \right)}_{\text{smp}(p,\mu)} \right)}_{\text{smp}(p,\mu)} \\ \underbrace{I_m \otimes A_n}_{\text{smp}(p,\mu)} \to I_p \otimes_{\parallel} \left(I_{m/p} \otimes A_n \right) \\ \underbrace{\left(P \otimes I_n \right)}_{\text{smp}(p,\mu)} \to \left(P \otimes I_{n/\mu} \right) \overline{\otimes} I_{\mu} \\ \end{aligned}$$

SpiralGen

Simple Rewriting Example

Hardware Generation for Performance



Software/Hardware Generation for Performance



Parallelization by Rewriting

$$\underbrace{\operatorname{DFT}_{mn}}_{\operatorname{smp}(p,\mu)} \rightarrow \underbrace{\left((\operatorname{DFT}_{m} \otimes \operatorname{I}_{n}) \operatorname{T}_{n}^{mn} (\operatorname{I}_{m} \otimes \operatorname{DFT}_{n}) \operatorname{L}_{m}^{mn} \right)}_{\operatorname{smp}(p,\mu)} \\
\cdots \\
\rightarrow \underbrace{\left(\operatorname{DFT}_{m} \otimes \operatorname{I}_{n} \right)}_{\operatorname{smp}(p,\mu)} \underbrace{\operatorname{T}_{n}^{mn}}_{\operatorname{smp}(p,\mu)} \underbrace{\left(\operatorname{I}_{m} \otimes \operatorname{DFT}_{n} \right)}_{\operatorname{smp}(p,\mu)} \underbrace{\operatorname{L}_{m}^{nm}}_{\operatorname{smp}(p,\mu)} \\
\cdots \\
\rightarrow \left((\operatorname{L}_{m}^{mp} \otimes \operatorname{I}_{n/p\mu}) \overline{\otimes} \operatorname{I}_{\mu} \right) \left(\operatorname{I}_{p} \otimes || (\operatorname{DFT}_{m} \otimes \operatorname{I}_{n/p}) \right) \left((\operatorname{L}_{p}^{mp} \otimes \operatorname{I}_{n/p\mu}) \overline{\otimes} \operatorname{I}_{\mu} \right) \\
\underbrace{\left(\bigcup_{i=0}^{p-1} \operatorname{T}_{n}^{mn,i} \right)}_{i=0} \left(\operatorname{I}_{p} \otimes || (\operatorname{I}_{m/p} \otimes \operatorname{DFT}_{n}) \right) \left(\operatorname{I}_{p} \otimes || \operatorname{L}_{m/p}^{mn/p} \right) \left((\operatorname{L}_{p}^{pn} \otimes \operatorname{I}_{m/p\mu}) \overline{\otimes} \operatorname{I}_{\mu} \right) \\$$

Fully optimized (load-balanced, no false sharing) in the sense of our definition



Same Approach for Other Parallel Paradigms

Message Passing:

$\underbrace{\mathbf{DFT}_{mn}}_{msg(p,\mu)}$	\rightarrow	$\underbrace{\left((\mathbf{DFT}_m\otimes \mathbf{I}_n)T_n^{mn}(\mathbf{I}_m\otimes \mathbf{DFT}_n)L_m^{mn}\right)}_{msg(p,\mu)}$
	• • •	
	\rightarrow	$\underbrace{\left(\mathbf{DFT}_{m}\otimes\mathbf{I}_{n}\right)}_{msg(p,\mu)}\underbrace{T_{n}^{mn}}_{msg(p,\mu)}\underbrace{\left(\mathbf{I}_{m}\otimes\mathbf{DFT}_{n}\right)}_{msg(p,\mu)}\underbrace{L_{m}^{nm}}_{msg(p,\mu)}$
	• • •	
	\rightarrow	$\left((L_m^{mp}\otimes \mathrm{I}_{n/p\mu})\bar{\otimes}\mathrm{I}_{\mu}\right)\left(\mathrm{I}_p\otimes_{\parallel}(\mathbf{DFT}_m\otimes \mathrm{I}_{n/p})\right)\left((L_p^{mp}\otimes \mathrm{I}_{n/p\mu})\bar{\otimes}\mathrm{I}_{\mu}\right)$
		$\left(\bigoplus_{i=0}^{p-1} T_n^{mn,i}\right) \Big(\mathrm{I}_p \otimes_{\parallel} (\mathrm{I}_{m/p} \otimes \mathbf{DFT}_n) \Big) \Big(\mathrm{I}_p \otimes_{\parallel} L_{m/p}^{mn/p} \Big) \Big((L_p^{pn} \otimes \mathrm{I}_{m/p\mu}) \bar{\otimes} \mathrm{I}_{\mu} \Big)$

Vectorization:



GPUs:

$$\underbrace{\begin{pmatrix} \mathbf{DFT}_{rk} \\ gpu(t,c) \end{pmatrix}}_{gpu(t,c)} \rightarrow \underbrace{\begin{pmatrix} \prod_{i=0}^{k-1} \mathsf{L}_{r}^{r^{k}} \left(\mathbf{I}_{r^{k-1}} \otimes \mathbf{DFT}_{r} \right) \left(\mathsf{L}_{r^{k-i-1}}^{r^{k}} (\mathbf{I}_{r^{i}} \otimes \mathsf{T}_{r^{k-i-1}}^{r^{k-i}}) \underbrace{\mathsf{L}_{r^{i+1}}^{r^{k}}}_{\operatorname{vec}(c)} \right) }_{gpu(t,c)} \\ \cdots \\ \rightarrow \underbrace{\begin{pmatrix} \prod_{i=0}^{k-1} (\mathsf{L}_{r}^{r^{n}/2} \vec{\otimes} \mathbf{I}_{2}) \left(\mathbf{I}_{r^{n-1}/2} \otimes \times \underbrace{(\mathbf{DFT}_{r} \vec{\otimes} \mathbf{I}_{2}) \mathsf{L}_{r}^{2r}}_{\operatorname{shd}(t,c)} \right) \mathsf{T}_{i} \\ (\mathsf{L}_{r}^{r^{n}/2} \vec{\otimes} \mathbf{I}_{2}) (\mathbf{I}_{r^{n-1}/2} \otimes \times \underbrace{\mathsf{L}_{r}^{2r}}_{\operatorname{shd}(t,c)}) (\mathsf{R}_{r}^{r^{n-1}} \vec{\otimes} \mathbf{I}_{r}) \end{aligned}}$$

Verilog for FPGAs:

$$\underbrace{ \begin{pmatrix} \mathbf{DFT}_{rk} \\ \mathbf{Stream}(r^{s}) \end{pmatrix}}_{\mathsf{stream}(r^{s})} \rightarrow \underbrace{ \begin{bmatrix} \prod_{i=0}^{k-1} \mathsf{L}_{r}^{rk} \left(\mathbf{I}_{rk-1} \otimes \mathbf{DFT}_{r} \right) \left(\mathsf{L}_{rk-i-1}^{rk} (\mathbf{I}_{ri} \otimes \mathsf{T}_{rk-i-1}^{rk-i}) \mathsf{L}_{ri+1}^{rk} \right) \end{bmatrix} \mathsf{R}_{r}^{rk}}_{\mathsf{stream}(r^{s})} \\ \cdots \\ \rightarrow \underbrace{ \begin{bmatrix} k-1 \\ \prod_{i=0}^{k-1} \underbrace{\mathsf{L}_{r}^{rk}}_{\mathsf{stream}(r^{s})} \underbrace{ \left(\mathbf{I}_{rk-1} \otimes \mathbf{DFT}_{r} \right) }_{\mathsf{stream}(r^{s})} \underbrace{ \left(\mathsf{L}_{rk-i-1}^{rk} (\mathbf{I}_{ri} \otimes \mathsf{T}_{rk-i-1}^{rk-i}) \mathsf{L}_{ri+1}^{rk} \right) }_{\mathsf{stream}(r^{s})} \end{bmatrix} \underbrace{ \mathsf{R}_{r}^{rk}}_{\mathsf{stream}(r^{s})} \\ \cdots \\ \rightarrow \underbrace{ \begin{bmatrix} k-1 \\ \prod_{i=0}^{k-1} \underbrace{\mathsf{L}_{r}^{rk}}_{\mathsf{stream}(r^{s})} \left(\mathbf{I}_{rk-s-1} \otimes s(\mathbf{I}_{rs-1} \otimes \mathbf{DFT}_{r}) \right) \underbrace{\mathsf{T}_{i}'}_{\mathsf{stream}(r^{s})} \end{bmatrix} \underbrace{ \mathsf{R}_{r}^{rk}}_{\mathsf{stream}(r^{s})} \\ \underbrace{ \mathsf{R}_{r}^{rk}}_{\mathsf{stream}(r^{s})} \underbrace{ \mathsf{R}_{r}^{rk}}$$

- Rigorous, correct by construction
- Overcomes compiler limitations

Carnegie Mellon

SpiralGen

Software/Hardware Generation for Performance

🕏 Spiral

Autotuning in Constraint Solution Space



Carnegie Mellon





Translating an OL Expression Into Code





Discussion

- Parallelization at the mathematical level through rewriting and constraint programming
- Generates a space of "reasonable algorithms" that can be searched for adaptation to memory hierarchy
- Very efficient since no analysis is required
- Principled, domain-specific approach
- Applicable across transforms and parallelism types



Spiral<mark>Gen</mark>

Message Passing

re/Hardware Generation for Performance

Good construct: tensor product

$$y = (\mathbf{I}_p \otimes A) x$$

Characteristics: no communication



• Permutations are explicit communication $y = (L_2^4 \otimes I_2)x$





Apply same 3-step approach: 1. Identify hw parameters

- **2.** Identify good formulas

Х

3. Identify rewriting rules

Software/Hardware Generation for Performance



Parallelization for Distributed Memory

$$\underbrace{\mathsf{DFT}_{mn}}_{\mathsf{par}(p)} \rightarrow \underbrace{(\mathsf{DFT}_{m} \otimes \mathbf{I}_{n})}_{\mathsf{par}(p \leftarrow q)} \underbrace{\mathsf{T}_{n}^{mn}}_{\mathsf{par}(q)} \underbrace{(\mathbf{I}_{m} \otimes \mathsf{DFT}_{n})}_{\mathsf{par}(q)} \underbrace{\mathsf{L}_{m}^{mn}}_{\mathsf{par}(q \leftarrow p)} \\ \dots \\ \dots \\ \dots \\ \rightarrow \underbrace{(\mathbf{I}_{p} \otimes_{\parallel} \mathsf{L}_{m/p}^{mn/p})}_{\mathsf{C}} \underbrace{(\mathsf{L}_{p}^{p^{2}} \otimes \mathbf{I}_{mn/p^{2}})}_{\mathsf{comm}(p \leftarrow q)} \underbrace{(\mathbf{I}_{q} \otimes_{\parallel} (\mathbf{I}_{p/q} \otimes \mathsf{L}_{p}^{n} \otimes \mathbf{I}_{m/p}))(\mathbf{I}_{q} \otimes_{\parallel} (\mathbf{I}_{n/q} \otimes \mathsf{DFT}_{m}))}_{\mathsf{C}} \\ \underbrace{(\mathbf{I}_{q} \otimes_{\parallel} \mathsf{L}_{m/q}^{mn/q})}_{\mathsf{comm}(q)} \underbrace{(\mathsf{L}_{q}^{q^{2}} \otimes \mathbf{I}_{mn/q^{2}})}_{\mathsf{comm}(q)} \underbrace{(\mathbf{I}_{q} \otimes_{\parallel} (\mathsf{L}_{q}^{n} \otimes \mathbf{I}_{m/q}))\mathsf{T}_{n}^{mn} (\mathsf{I}_{q} \otimes_{\parallel} (\mathbf{I}_{m/q} \otimes \mathsf{DFT}_{n}))}_{\mathsf{comm}(q \leftarrow p)} \underbrace{(\mathbf{I}_{q} \otimes_{\parallel} (\mathsf{L}_{p/q} \otimes \mathsf{L}_{m/p}^{mn/p}))}_{\mathsf{comm}(q \leftarrow p)} \underbrace{(\mathsf{I}_{p} \otimes_{\parallel} (\mathsf{L}_{p/p} \otimes \mathsf{I}_{m/p}))}_{\mathsf{comm}(q \leftarrow p)} \underbrace{(\mathsf{I}_{p/p} \otimes \mathsf{I}_{m/p})}_{\mathsf{comm}(q \leftarrow p)} \underbrace{\mathsf{I}_{m/p}} \underbrace{(\mathsf$$

p-way parallelized with intermediate computation on *q* processors



Data streams steadily in packets



Apply same 3-step approach: 1. Identify hw parameters

- **2.** Identify good formulas
- Identify rewriting rules **3**.

Carnegie Mellon

Spiral<mark>Gen</mark>

Carnegie Mellon



Streaming by Rewriting

$$\underbrace{\begin{pmatrix} \mathbf{DFT}_{rk} \\ \mathsf{stream}(r^{s}) \end{pmatrix}}_{\mathsf{stream}(r^{s})} \rightarrow \underbrace{\begin{bmatrix} \lim_{i=0}^{k-1} \mathsf{L}_{r}^{rk} \left(\mathbf{I}_{rk-1} \otimes \mathbf{DFT}_{r} \right) \left(\mathsf{L}_{rk-i-1}^{rk} (\mathbf{I}_{ri} \otimes \mathsf{T}_{rk-i-1}^{rk-i}) \mathsf{L}_{ri+1}^{rk} \right) \right] \mathsf{R}_{r}^{rk}}_{\mathsf{stream}(r^{s})} \\ \cdots \\ \rightarrow \underbrace{\begin{bmatrix} \lim_{i=0}^{k-1} \underbrace{\mathsf{L}_{r}^{rk}}_{\mathsf{stream}(r^{s})} \left(\underbrace{\mathbf{I}_{rk-1} \otimes \mathbf{DFT}_{r}}_{\mathsf{stream}(r^{s})} \left(\underbrace{\mathsf{L}_{rk-i-1}^{rk} (\mathbf{I}_{ri} \otimes \mathsf{T}_{rk-i-1}^{rk-i}) \mathsf{L}_{ri+1}^{rk}}_{\mathsf{stream}(r^{s})} \right) \right] \underbrace{\mathsf{R}_{r}^{rk}}_{\mathsf{stream}(r^{s})} \\ \cdots \\ \rightarrow \underbrace{\begin{bmatrix} \lim_{i=0}^{k-1} \underbrace{\mathsf{L}_{r}^{rk}}_{\mathsf{stream}(r^{s})} \left(\underbrace{\mathbf{I}_{rk-1} \otimes \mathbf{DFT}_{r}}_{\mathsf{stream}(r^{s})} \otimes \mathbf{DFT}_{r} \right) \right) \underbrace{\mathsf{T}_{i}^{rk}}_{\mathsf{stream}(r^{s})} \\ \end{bmatrix} \underbrace{\mathsf{R}_{r}^{rk}}_{\mathsf{stream}(r^{s})} \underbrace{\mathsf{R}_{r}^{rk}}_{\mathsf$$

streamed at r^s words per cycle

base cases

É

Software/Hardware Generation for Performance





Target: Specialized Soft Processor



Hardware design issue → SPIRAL algorithm transformation + C coding style issue

Carnegie Mellon

SpiralGen

Software/Hardware Generation for Performance

OpenCL State Machine Code Generation

```
DFT<sub>8</sub>
          \checkmark
                                           \sum_{i3=0}^{1} \left(\sum_{i6=0}^{1} S_{2,i6} A_2 G_{2,i6} \cdot \sum_{i7=0}^{1} S_{1,i7} A_1 G_{1,i7}\right) \cdot \sum_{i9=0}^{3} S_{0,i2} A_0 G_{0,i2}
    DFT_2 DFT_4
           DFT_2 DFT_2
                                                                          while (true) {
                                                                               if (bben0==1 && i2<=3) {</pre>
                                                                                    // output logic
                                                                                    output = f(i2);
                                                                                    // next state logic
                                                                                    if (i2<3) {
for(int i2 = 0; i2 <= 3; i2++) {</pre>
                                                                                        i2++;
                                                                                    } else if (i2==3) {
     BB(0);
                                                                                        i2=0; bben0=0;
}
                                                                                       bben1=1;
for(int i3 = 0; i3 <= 1; i3++) {</pre>
                                                                                    1
     for(int i7 = 0; i7 <= 1; i7++) {</pre>
                                                                               else if (bben1==1 && i7<=1) {</pre>
           BB(1);
                                                                                    // output logic
     }
                                                                                    // next state logic
     for(int i6 = 0; i6 <= 1; i6++) {</pre>
                                                                               }
                                                                               else if (bben2==1 && i6<=1) {</pre>
           BB(2);
                                                                                    // output logic
     }
                                                                                    // next state logic
                                                                                write channel(ouput);
                                                                          }
```



Organization

are/Hardware Generation for Performance

- SPL: Problem and algorithm specification
- **Σ-SPL:** Automating high level optimization
- Rewriting: Formal parallelization
- Rewriting: Vectorization
- Verification
- Spiral as FFTX backend
- Summary

F. Franchetti, M. Püschel

Short Vector Code Generation for the Discrete Fourier Transform

Proceedings of the 17th International Parallel and Distributed Processing Symposium (IPDPS '03), pages 58-67.

F. Franchetti and M. Püschel Generating SIMD Vectorized Permutations Proceedings of International Conference on Compiler Construction (CC) 2008



Spiral<mark>Gen</mark>

Software/Hardware Generation for Performance SIMD (Signal Instruction Multiple Data) Vector Instructions in a Nutshell

What are these instructions?

Extension of the ISA. Data types and instructions for parallel computation on short (2-way–16-way) vectors of integers and floats



Problems:

- Not standardized
- Compiler vectorization limited
- Low-level issues (data alignment,...)
- Reordering data kills runtime

Intel MMX

- AMD 3DNow!
- Intel SSE
- AMD Enhanced 3DNow!
- Motorola AltiVec/VMX
- AMD 3DNow! Professional
- Intel SSE2
- IBM BlueGene/L PPC440FP2
- IBM QPX
- IBM VSX
- Intel SSE3
- Intel SSSE3
- Intel SSE4, 4.1, 4.2
- Intel AVX, AVX2
- Intel AVX512

One can easily slow down a program by vectorizing it





Vectorization: Basic Idea

Good construct: tensor product

$$y = \left(A \otimes \mathbf{I}_{\nu}\right) x$$



Characteristics: block operation and alignment preserving

Problematic construct: permutations must be done in register



Task: Rewrite formulas to extract tensor product + minimize in-register shuffles

Carnegie Mellon



SIMD Vectorization: 3-Step Procedure

- Identify crucial hardware parameters A_{\sim} 1. $vec(\nu)$
 - **Vector length:** v
- 2. Identify good formulas
 - Tensor product: $A \otimes I_{\nu}$
 - Base cases: Build library from shuffle instructions unpacklo, unpackhi, shufps,...
 - **Definition:** Vectorized formula
- 3. Identify rewriting rules



Software/Hardware Generation for Performance



Vectorization by Rewriting



Formula is vectorized w.r.t. Definition



ware/Hardware Generation for Performance



Vectorization of Odd Problem Sizes

Zero-padding: Load/store km elements into/from m v-way vectors





SPL formula	data type	compiled to
$ \begin{array}{l} \mathbf{I}_{k \times 4} \\ \mathbf{I}_{4 \times k} \\ \mathbf{I}_{k \times 8} \\ \mathbf{I}_{8 \times k} \end{array} $	4-way float 4-way float 8-way short 8-way short	_mm_maskmoveu_si128 + _mm_castps_si128 _mm_loadu_ps + _mm_and_i128 _mm_maskmoveu_si128 _mm_loadu_si128



Automatically Deriving Vector Base Cases



- Translate SIMD vector ISA into matrix representation
- Design rule system to generate vector matrix formulas
- Define cost measure on matrix formulas
- Use dynamic programming with backtracking to find vector program with minimal cost

Vector matrix formula in BNF

$$\begin{array}{ll} \langle \mathrm{vmf} \rangle & ::= & \langle \mathrm{vmf} \rangle \langle \mathrm{vmf} \rangle \mid \mathrm{I}_m \otimes \langle \mathrm{vmf} \rangle \mid \begin{pmatrix} \langle \mathrm{vmf} \rangle \\ \langle \mathrm{vmf} \rangle \end{pmatrix} \mid \langle \mathrm{perm} \rangle \otimes \mathrm{I}_{\nu} \mid \\ & \langle \mathrm{perm} \rangle \otimes \mathrm{I}_{\nu/2} \text{ if } \mathrm{L}_2^4 \otimes \mathrm{I}_{\nu/2} \text{ possible} \mid M_{\mathrm{instr}} \text{ with instr in ISA} \\ & \langle \mathrm{perm} \rangle & ::= & \mathrm{L}_m^{mn} \mid \mathrm{I}_m \otimes \langle \mathrm{perm} \rangle \mid \langle \mathrm{perm} \rangle \otimes \mathrm{I}_m \mid \langle \mathrm{perm} \rangle \langle \mathrm{perm} \rangle \end{array}$$

11

 \sim



Spiral<mark>Gen</mark>

Software/Hardware Generation for Performance

Translating Instructions into Matrices

```
Intel C++ Compiler Manual
__m128 _mm_unpackhi_ps(__m128 a, __m128 b)
r0 := a2; r1 := b2; r2 := a3; r3 := b3
```

Instruction specification (GAP code)

```
Intel_SSE2.4_x_float._mm_unpackhi_ps := rec(
    v := 4,
    semantics := (a, b, p) -> [a[2], b[2], a[3], b[3]],
    parameters := []
);
```

Automatically build matrix from semantics () function

Carnegie Mellon



Example: Sequence of Two Instructions





Rule System: Recursive Matrix Factorization

- Recursively factorizes stride permutations
- "Blocking of matrix transposition" in linear memory
- Choices -> Dynamic programming with backtracking
- Trigger ISA-specific termination rules





Cost Function: Weighted Instruction Count

- Defines recursive cost function for matrix formulas
- Each instruction has an associated cost
- Vector assignments are "for free"



Carnegie Mellon

ardware Generation for Performance



64 Vector Program: 8-way Vectorized L_8^{o}

```
 \mathsf{L}_8^{64} \ = \ \big( \operatorname{I}_4 \otimes (\mathsf{L}_2^4 \otimes \operatorname{I}_4) \big) \big( \operatorname{L}_4^8 \otimes \operatorname{I}_8 \big) \big( \operatorname{I}_4 \otimes (\mathsf{L}_4^8 \otimes \operatorname{I}_2) \big) \big( (\operatorname{I}_2 \otimes \mathsf{L}_2^4) \otimes \operatorname{I}_8 \big) \big( \operatorname{I}_4 \otimes \mathsf{L}_8^{16} \big)
```

```
m128 X[8], Y[8], t3, t4, t7, t8, t11, t12, t15, t16,
      t17, t18, t19, t20, t21, t22, t23, t24;
t3 = mm unpacklo epi16(X[0], X[1]); t4 = mm unpackhi epi16(X[0], X[1]);
t7 = mm unpacklo epi16(X[2], X[3]); t8 = mm unpackhi epi16(X[2], X[3]);
t11 = mm unpacklo epi16(X[4], X[5]); t12 = mm unpackhi epi16(X[4], X[5]);
t15 = mm unpacklo epi16(X[6], X[7]); t16 = mm unpackhi epi16(X[6], X[7]);
t17 = mm unpacklo epi32(t3, t7); t18 = mm unpackhi epi32(t3, t7);
t19 = mm unpacklo epi32(t4, t8); t20 = mm unpackhi epi32(t4, t8);
t21 = mm unpacklo epi32(t11, t15); t22 = mm unpackhi epi32(t11, t15);
t23 = mm unpacklo epi32(t12, t16); t24 = mm unpackhi epi32(t12, t16);
Y[0] = mm unpacklo epi64(t17, t21); Y[1] = mm unpackhi epi64(t17, t21);
Y[2] = mm unpacklo epi64(t18, t22); Y[3] = mm unpackhi epi64(t18, t22);
Y[4] = mm unpacklo epi64(t19, t23); Y[5] = mm unpackhi epi64(t19, t23);
Y[6] = mm unpacklo epi64(t20, t24); Y[7] = mm unpackhi epi64(t20, t24);
```

8-way vectorized transposition of 8x8 matrix



Organization

vare/Hardware Generation for Performance

- SPL: Problem and algorithm specification
- **Σ-SPL:** Automating high level optimization
- Rewriting: Formal parallelization
- Rewriting: Vectorization
- Verification
- Spiral as FFTX backend
- Summary



Symbolic Verification

/Hardware Generation for Perfor

Transform = Matrix-vector multiplication matrix fully defines the operation

$$\mathsf{DFT}_4 = \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & j & -1 & -j \\ 1 & -1 & 1 & -1 \\ 1 & -j & -1 & j \end{bmatrix}$$

Algorithm = Formula represents a matrix expression, can be evaluated to a matrix

$$(\mathsf{DFT}_2 \otimes I_2) \mathsf{T}_2^4(I_2 \otimes \mathsf{DFT}_2) \mathsf{L}_2^4 = \begin{bmatrix} 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \\ 1 & 0 & -1 & 0 \\ 0 & 1 & 0 & -1 \end{bmatrix} \begin{bmatrix} 1 & 1 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & 1 \\ 0 & 0 & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & j \end{bmatrix} \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}$$



Empirical Verification

 Run program on all basis vectors, compare to columns of transform matrix



 Compare program output on random vectors to output of a random implementation of same kernel

DFT4([0.1,1.77,2.28,-55.3]) = = ? DFT4 rnd([0.1,1.77,2.28,-55.3])




Verification of the Generator

 Rule replaces left-hand side by right-hand side when preconditions match

$$\mathbf{I}_m \otimes A_n \to \mathsf{L}_m^{mn}(A_n \otimes \mathbf{I}_m) \,\mathsf{L}_n^{mn}$$

 Test rule by evaluating expressions before and after rule application and compare result



Organization

vare/Hardware Generation for Performance

- SPL: Problem and algorithm specification
- **Σ-SPL:** Automating high level optimization
- Rewriting: Formal parallelization
- Rewriting: Vectorization
- Verification
- Spiral as FFTX backend
- Summary





Have You Ever Wondered About This?





Spectral Algorithms

No LAPACK equivalent for spectral methods

- Medium size 1D FFT (1k—10k data points) is most common library call applications break down 3D problems themselves and then call the 1D FFT library
- Higher level FFT calls rarely used
 FFTW guru interface is powerful but hard to used, leading to performance loss
- Low arithmetic intensity and variation of FFT use make library approach hard Algorithm specific decompositions and FFT calls intertwined with non-FFT code

Software/Hardware Generation for Performance



FFTX and SpectralPACK: Long Term Vision



Spectral Algorithms



Define the LAPACK equivalent for spectral algorithms

- Define FFTX as the BLAS equivalent provide user FFT functionality as well as algorithm building blocks
- Define class of numerical algorithms to be supported by SpectralPACK
 PDE solver classes (Green's function, sparse in normal/k space,...), signal processing,...
- Define SpectralPACK functions circular convolutions, NUFFT, Poisson solvers, free space convolution,...

FFTX and SpectralPACK solve the "spectral dwarf" long term





Example: Hockney Free Space Convolution















Example: Hockney Free Space Convolution

```
fftx plan pruned real convolution plan(fftx real *in, fftx real *out, fftx complex *symbol,
        int n, int n in, int n out, int n freq) {
    int rank = 1,
    batch rank = 0,
    . . .
    fftx plan plans[5];
    fftx plan p;
    tmp1 = fftx create zero temp real(rank, &padded dims);
   plans[0] = fftx plan guru copy real(rank, &in dimx, in, tmp1, MY FFTX MODE SUB);
    tmp2 = fftx create temp complex(rank, &freq dims);
   plans[1] = fftx plan guru dft r2c(rank, &padded dims, batch rank,
        &batch dims, tmp1, tmp2, MY FFTX MODE SUB);
    tmp3 = fftx create temp complex(rank, &freq dims);
    plans[2] = fftx plan guru pointwise c2c(rank, & freq dimx, batch rank, & batch dimx,
        tmp2, tmp3, symbol, (fftx callback)complex scaling,
        MY FFTX MODE SUB | FFTX PW POINTWISE);
    tmp4 = fftx create temp real(rank, &padded dims);
   plans[3] = fftx plan guru dft c2r(rank, &padded dims, batch rank,
        &batch dims, tmp3, tmp4, MY FFTX MODE SUB);
   plans[4] = fftx plan guru copy real(rank, &out dimx, tmp4, out, MY FFTX MODE SUB);
   p = fftx plan compose(numsubplans, plans, MY FFTX MODE TOP);
```

return p;

}

Looks like FFTW calls, but is a specification for SPIRAL

Spiral**Gen**



FFTX Backend: SPIRAL



```
Software/Hardware Generation for Performance
```





1,000s of lines of code, cross call optimization, etc., transparently used

F. Franchetti, D. G. Spampinato, A. Kulkarni, D. T. Popovici, T. M. Low, M. Franusich, A. Canning, P. McCorquodale, B. Van Straalen, P. Colella: **FFTX and SpectralPack: A First Look**, IEEE International Conference on High Performance Computing, Data, and Analytics (HiPC), 2018



Organization

vare/Hardware Generation for Performance

- SPL: Problem and algorithm specification
- **Σ-SPL:** Automating high level optimization
- Rewriting: Formal parallelization
- Rewriting: Vectorization
- Verification
- Spiral as FFTX backend
- Summary

Spiral Software/Hardware Generation for Performance

Co-Optimizing Architecture and Kernel





QED.

Software/Hardware Generation for Performance

piral



High Assurance Spiral

Equations of Motion



 $v_r = \dot{x}, \quad 0 < v_r < V$ $a = \dot{v_r}, \quad -b < a < A$

Safety condition



 $v_r = \dot{x}, \quad 0 < v_r < V$

 $a = v_r, \quad -b < a < A$

KeYmaera

Hybrid Theorem Prover

F. Franchetti, T. M. Low, S. Mitsch, J. P. Mendoza, L. Gui, A. Phaosawasdi, D. Padua, S. Kar, J. M. F. Moura, M. Franusich, J. Johnson, A. Platzer, and M. Veloso High-Assurance SPIRAL: End-to-End Guarantees for Robot and Car Control IEEE Control Systems Magazine, 2017, pages 82-103.





General Size Library Generation Input:

- **Transform**: DFT_n
- Algorithms: $\mathrm{DFT}_{km} \to (\mathrm{DFT}_k \otimes I_m) T_m^{km} (I_k \otimes \mathrm{DFT}_m) L_k^{km}$ $\mathrm{DFT}_2 \to \begin{bmatrix} 1 & -1 \\ 1 & -1 \end{bmatrix}$
- Vectorization: 2-way SSE
- Threading: Yes

Output:

- Optimized library (10,000 lines of C++)
- For general input size
 (not collection of fixed sizes)
- Vectorized
- Multithreaded
- With runtime adaptation mechanism
- Performance competitive with hand-written code

Yevgen Voronenko, Frédéric de Mesmay and Markus Püschel Computer Generation of General Size Linear Transform Libraries Proc. International Symposium on Code Generation and Optimization (CGO), pp. 102-113, 2009





Graph Algorithms in SPIRAL

Foundation







Formalization

Operation	Mathematical Description	Output	Inputs
mxm	$\mathbf{C} \langle \mathbf{\neg M}, \mathbf{z} \rangle \ = \mathbf{C} \ \odot \ (\mathbf{A}^{T} \oplus . \otimes \mathbf{B}^{T})$	С	¬, M, z, ⊙, A, T, ⊕.⊗, B, T
mxv, (vxm)	$\mathbf{c}\langle \neg \mathbf{m}, \mathbf{z} \rangle = \mathbf{c} \odot (\mathbf{A}^{T} \oplus \otimes \mathbf{b})$	с	¬, m, z, ⊙, A, T, ⊕.⊗, b
eWiseMult	$C\langle \neg M, z \rangle = C \odot (A^T \otimes B^T)$	С	¬, M, z, ⊙, A, T, ⊗, B, T
eWiseAdd	$C\langle \neg M, z \rangle = C \odot (A^T \oplus B^T)$	С	¬, M, z, ⊙, A, T, ⊕, B, T
reduce (row)	c⟨¬m, z⟩ = c ⊙ [⊕ _j A ^T (:,j)]	с	¬, m, z, ⊙, A, T, ⊕
apply	$\mathbf{C}\langle \mathbf{\neg M}, \mathbf{z} \rangle = \mathbf{C} \odot f(\mathbf{A}^{T})$	С	¬, M, z, ⊙, A, T , f
transpose	$C\langle \neg M, z \rangle = C \odot A^T$	С	¬, M, z, ⊙, A (T)
extract	$C\langle \neg M, z \rangle = C \odot A^{T}(i,j)$	С	¬, M, z, ⊙, A, T, i, j
assign	$C\langle TM, z \rangle$ (i,j) = $C(i,j) \odot A^{T}$	С	¬, M, z, ⊙, A, T, i, j
build (meth.)	$\textbf{C} = \$^{m \times n}(\textbf{i},\textbf{j},\textbf{v},\odot)$	С	⊙, m, n, i , j , v
extractTuples (meth.)	$(\mathbf{i},\mathbf{j},\mathbf{v}) = \mathbf{A}$	i,j,v	А

Notation: i,j – index arrays, v – scalar array, m – 1D mask, other bold-lower – vector (column), M – 2D mask, other bold-caps – matrix, T – transpose, ¬ - structural complement, z – clear output, \oplus monoid/binary function, \oplus . \otimes semiring, blue – optional parameters, red – optional modifiers

In collaboration with CMU-SEI

Context

- Kepner & Gilbert et al recast graph algorithms as linear algebra operations
- GraphBLAS Forum and reference implementations
- IBM, Intel, national labs etc. on board

HIVE Graph Challenge

	First Look: Linear Al Counting without M	lgebra-Based Triangle Iatrix Multiplication
allenge Champions	Tze Meng Low, Varun Nagaraj Rao, Matthew Lee, Doru Department of Electrical and Computer E Carnegie Meliou University Email: lowt@cma.edu, vntao@andrew.cma.edu, (matthf, o	Popovici, Franz Franchetti Scott McMillan ngineering Software Engineering Institute Carnegie Melhou University popovic, franzf]@cma.edu Email: smemillan@sei.ema.edu
skyhork medin Toongo Constra on ink Kalakan Toola, Mishak Wali, Mahana Dowei, Jonathan Barry, Smon Menaheran Salamatan Salamatan Salamatan Salamatan Salamatan Salamatan Salamatan Salamatan Leng Denga Common Salamatan Salamatan Salamatan Mahanan Mahayamatan (2013), Akasah Ana Yang Mahanan Tamang POND and Yang Ang Ang Ang Ang Ang Ang Ang Ang Ang A	Abreat— Linear algebra-haved approaches to exact triangle counting edten require queue matrix multiplication as a primitive entries. Non-linear algebra approaches to the same problem smallele. In this process when the this approaches not multiplication of the process when the this approaches not multiplication of the process when the this approaches not algebra has in the process when the this approaches not algebra has income to multiplication. Allowed and algebra has income to multiplication and and the same entries and triangle exerting ones can be destined. In addition, that the same algebra in explorible in the competierement	Finally, we show that our implementation of exact tri- angle compite physicher yields exponsing performance that is between 00 and new that 2000 times that that the reference implementation. Initial parallelation effort yields an additional factor of 12 to 15.71 meyorement over the sequential implementation on strates architectures. III. A FAUNAEL CONSTING ACCOMPTION Let $(J = U, E)$ be a simple understod graph with vertex set V and edge at E . In addition, and much V has been
upoation on Shareb Mennery Parullel Systems - Shadan Smith (UMN; hats), Xing Lin, Nauson K. Ahmed (Iatal), Anoy (XDD), Palatiah Petrisi (Iatal), George Karyja (CXDD) iomatram, Sensorn Ahmed, Shaden Smith, Shija Eyerman, Milhundundra Kodyath, Breahin Her, Paletisio Petrisi (Intal), and CMD).	algorithm attained assuming that the adjacency matrix of the graph is not available, We shew that our approach yields an initial implementation that is between 60 and more than 3000 the initial implementation can be easily parallelized on shared memory systems.	partitioned into two disjoint sets, V_{TL} and V_{TD} . Under these assumptions, a triangle is G , described uning the 3-tuple (u, v, w) where $u, v, w \in V$, can be classified into four categories: - Category 1: Thirapple in V_{TL} . Vertices of these triangles are from V_{V-L} is $u, v, w \in V_{V-}$.
yn Contrig Je Connting of Extreme Scale - Yang Hu, Pradsep Kamar (GWU), Guy Swope (Raythean), H. Howie Huang (GWU) arda	I. INTRODUCTION It is generally known that counting the exact number of triangles in a graph G can be described using in the language	- Category 2: Triangles mostly in V_{TL} . Vertices of these triangles are form with two vertices in V_{TL} and one vertex in V_{BR} , i.e. $u, v \in V_{TL}$ and $w \in V_{BR}$.
e Praneucork for Detecting Community Changes in Dynamic Networks - Timothy La Fond, Geoffrey Staders, Christine S Endon Henson (LIXE) for a Thorac in Australa's Child Grans - Issues Ton - Form Yim (Georgis' Tech): Technical Branch Mind Resolution (Thir	of linear algebra as $\frac{1}{6}A^3$, where A is the utilization practice of the graph G III. Other	- Category 2: Triangles mostly in V_{BB} . Vertices of these triangles are form with one vertex in V_{TL} and two vertices in V_{BB} , i.e. $u \in V_{TL}$ and $v, w \in V_{BR}$.
ning u. Si na ori viringinano. Gono dreene, samar za originan nan (Orongin zona), Honro o manay, Honro o manay Hi Lakhrita, Shijie Zhou, Shreyso Singapara, Harqing Zeng, Rajgopal Karman, Vikite Prasama (USC), Dovid Bader ah)	linear algebra approaches [2], [3] also require a sparse-matrix multiplication of A or parts of A as part of their computation. Alternative approaches that are not based on linear algebra	 Category 4: Triangles in V_{BB}. Vertices of these triangles are from V_{BB}, i.e. u, v, w, ∈ V_{BB}. Figure 1 describes G and the four categories of triangles.
tion Awards	leverage other formats for describing graphs such as the adjacency list to design their adjacrithms [4], [5].	A. Intailine Let A be the error of (1) the number of simples where
ruus Decomposition on Multicore Systems - Humayun Kabir, Kamosh Madduri (Penn Stata)	ally exclusive. Using the linear algebra approaches are not multi-	vertices are all in Vrc (Category 1), and (2) the number of

 Preconditional Spactral Chattering for Stochastic Block Partition Streaming Graph Challenge - David Zhuzhanahvili (UC Bouldar), Andree Kranzer (Mitterhich Bestein: Bestech Laberezine (UEX))
 Daring and Implementation of Parallel Parallension in Mitterine Staffarmers. Shijis Zhon, Kariki Labhrita, Shonyan G. Singapara, Hamping Zang, Rajopak Kaman, Viktor Frasanna (USC), Jamas Par, Ean Kim, Odel Green, David Balse (Gorqia Tech)

Honorable Mention

An Ensen
 Klymko, 1

Graph C

- Distributed Triangle Counting in the Graphulo Matrix Math Library Dylan Hatthiaon (University of Washington)
 First Look: Linner-Algebre-Based Triangle Counting without Matrix Multiplication Tzu Mang Loo, Varun Nagaraj Rao, Matthew
 Jun Deen Remain: Even Teambolic (USU) Sett Molles of EU
- Lee, Deva Popovici, Franz Franchetti (CMU), Scott McMillan (SEJ) Scolable Stechanic Block Portition - Abasa Uppal (GWU), Guy Swopa (Raythson), and H. Howis Huang (GWU) (GWU)
- Sonahof Stochantz Back Partition Alison Uppal (UWU), Jong Yumpe (Kaythaen), and H. Howie Hanag (UWU) Soperatrider Association Array Architecture - Enk DuBandietis, Jeanine Cook (Sandia), Srisoshan Stilardh, Thomas Conte (Georgi Tech)
- Triangle Counting Via Vestorized Set Intersection Shakit Mowlari (Cuivernity of Pittsburgh) - Collaborative (CPU + GPU Algorithms for Triangle Counting and Trans Decomposition on the Missky Architecture - Katan Data, Keven Peng, Rohesh Nagi (UIUC), Jinjun Xiong (IBM), Num Sung Kim, Wen-Mei Hwu (UIUC)



SpiralGen Accelerating Innovation in Computing

SPIRAL FFTs in HPC/Supercomputing

- NCSA Blue Waters
 PAID Program, FFTs for Blue Waters
- RIKEN K computer
 FFTs for the HPC-ACE ISA
- LANL RoadRunner
 FFTs for the Cell processor
- PSC/XSEDE Bridges
 Large size FFTs
- LLNL BlueGene/L and P FFTW for BlueGene/L's Double FPU
- ANL BlueGene/Q Mira
 Early Science Program, FFTW for BGQ QPX











2006 Gordon Bell Prize (Peak Performance Award) with LLNL and IBM 2010 HPC Challenge Class II Award (Most Productive System) with ANL and IBM



BlueGene/P at Argonne National Laboratory 128k cores (quad-core CPUs) at 850 MHz

Software/Hardware Generation for Performance



Summary: Formal Code Synthesis

int dwmonitor(float *X, double *D) {

u2 = mm cvtps pd(mm addsub ps(

x2 = mm mul pd(x1, x6);

unsigned xm = mm getcsr();

u1 = _mm_set_pd(1.0, (-1.0));
for(int i5 = 0; i5 <= 2; i5++) {</pre>

u5 = mm set1 pd(0.0);

m128d u1, u2, u3, u4, u5, u6, u7, u8,..

mm setcsr(xm & 0xffff0000 | 0x0000dfc0)

mm set1 ps(FLT MIN), mm set1 ps(X[0])))

x6 = _mm_addsub_pd(_mm_set1_pd((DBL_MIN +DBL_MIN)), mm_loaddup_pd(&(D[i5])));

x1 = mm addsub pd(mm set1 pd(0.0), u1);















Hardware







performance

QED.





More Information: www.spiral.net www.spiralgen.com



Overview Papers

F. Franchetti, T. M. Low, D. T. Popovici, R. M. Veras, D. G. Spampinato, J. R. Johnson, M. Püschel, J. C. Hoe, J. M. F. Moura: **SPIRAL: Extreme Performance Portability,** Proceedings of the IEEE, Vol. 106, No. 11, 2018. Special Issue on *From High Level Specification to High Performance Code*

M. Püschel, F. Franchetti, Y. Voronenko: Spiral. Encyclopedia of Parallel Computing, D. A. Padua (Editor).

M. Püschel, J.M.F. Moura, J. Johnson, D. Padua, M. Veloso, B. Singer, J. Xiong, F. Franchetti, A. Gacic, Y. Voronenko, K. Chen, R.W. Johnson, and N. Rizzolo: **SPIRAL: Code Generation for DSP Transforms.** Special issue, Proceedings of the IEEE 93(2), 2005.

F. Franchetti, Y. Voronenko, S. Chellappa, J. M. F. Moura, and M. Püschel: **Discrete Fourier Transform on Multicores: Algorithms and Automatic Implementation.** IEEE Signal Processing Magazine, special issue on "Signal Processing on Platforms with Multiple Cores", 2009.

Core Technology Papers

F. Franchetti, F. de Mesmay, Daniel McFarlin, and M. Püschel: **Operator Language: A Program Generation Framework for Fast Kernels.** Proceedings of IFIP Working Conference on Domain Specific Languages (DSL WC), 2009.

Y. Voronenko, F. de Mesmay and M. Püschel: Computer Generation of General Size Linear Transform Libraries.

Proc. International Symposium on Code Generation and Optimization (CGO), pp. 102-113, 2009.

F. Franchetti, Y. Voronenko, M. Püschel: Loop Merging for Signal Transforms. Proceedings Programming Language Design and Implementation (PLDI) 2005, pages 315-326.

F. Franchetti, T. M. Low, S. Mitsch, J. P. Mendoza, L. Gui, A. Phaosawasdi, D. Padua, S. Kar, J. M. F. Moura, M. Franusich, J. Johnson, A. Platzer, and M. Veloso: **High-Assurance SPIRAL: End-to-End Guarantees for Robot and Car Control.** IEEE Control Systems Magazine, 2017, pages 82-103.

SIMD Vectorization

vare/Hardware Generation for Performance

F. Franchetti, M. Püschel: **Short Vector Code Generation for the Discrete Fourier Transform.** Proceedings of the 17th International Parallel and Distributed Processing Symposium (IPDPS '03), pages 58-67.

F. Franchetti, Y. Voronenko, M. Püschel: **A Rewriting System for the Vectorization of Signal Transforms.** Proceedings High Performance Computing for Computational Science (VECPAR) 2006, LNCS 4395, pages 363-377.

F. Franchetti and M. Püschel: **SIMD Vectorization of Non-Two-Power Sized FFTs.** Proceedings of International Conference on Acoustics, Speech, and Signal Processing (ICASSP) 07.

F. Franchetti and M. Püschel: **Generating SIMD Vectorized Permutations.** Proceedings of International Conference on Compiler Construction (CC) 2008.

D. S. McFarlin, V. Arbatov, F. Franchetti, M. Püschel: Automatic SIMD Vectorization of Fast Fourier Transforms for the Larrabee and AVX Instruction Sets. Proceedings of International Conference on Supercomputing (ICS), 2011.

Multicore and Distributed Memory

F. Franchetti, Y. Voronenko, and M. Püschel: **FFT Program Generation for Shared Memory: SMP and Multicore.** Proceedings Supercomputing 2006.

A. Bonelli, F. Franchetti, J. Lorenz, M. Püschel, and C. W. Ueberhuber: **Automatic Performance Optimization of the Discrete Fourier Transform on Distributed Memory Computers.** Proceedings of ISPA 06. Lecture Notes in Computer Science, Volume 4330, 2006, Pages 818 – 832.

S. Chellappa, F. Franchetti and M. Püschel: **Computer Generation of Fast FFTs for the Cell Broadband Engine.** Proceedings of International Conference on Supercomputing (ICS), 2009.

F. Franchetti, Y. Voronenko, and G. Almasi: Automatic Generation of the HPC Challenges Global FFT Benchmark for BlueGene/P. In Proceedings of High Performance Computing for Computational Science (VECPAR) 2012.

FPGA and Energy

ftware/Hardware Generation for Performance

P. A. Milder, F. Franchetti, J. C. Hoe, and M. Püschel: **Computer Generation of Hardware for Linear Digital Signal Processing Transforms.** ACM Transactions on Design Automation of Electronic Systems, 17(2), Article 15, 2012.

P. A. Milder, F. Franchetti, J. C. Hoe, and M. Püschel: **Formal Datapath Representation and Manipulation for Implementing DSP Transforms.** Proceedings of Design Automation Conference (DAC), 2008.

P. A. Milder, F. Franchetti, J. C. Hoe, and M. Püschel: Hardware Implementation of the Discrete Fourier Transform With Non-Power-Of-Two Problem Size. Proceedings of International Conference on Acoustics, Speech, and Signal Processing (ICASSP), 2010.

P. D'Alberto, F. Franchetti, P. A. Milder, A. Sandryhaila, J. C. Hoe, J. M. F. Moura, and M. Püschel: **Generating FPGA Accelerated DFT Libraries.** Proceedings of Field-Programmable Custom Computing Machines (FCCM) 2007.

B. Akin, P.A. Milder, F. Franchetti, and J. Hoe: **Memory Bandwidth Efficient Two-Dimensional Fast Fourier Transform Algorithm and Implementation for Large Problem Sizes.** IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM), 188-191, 2012.

B. Akin, F. Franchetti, J. Hoe: FFTs with Near-Optimal Memory Access Through Block Data Layouts. ICASSP 2014.

P. D'Alberto, M. Püschel, and F. Franchetti: **Performance/Energy Optimization of DSP Transforms on the XScale Processor.** Proceedings of International Conference on High Performance Embedded Architectures & Compilers (HiPEAC) 2007.



Applications (SAR and Software-Defined Radio)

D. McFarlin, F. Franchetti, M. Püschel, and J. M. F. Moura: **High Performance Synthetic Aperture Radar Image Formation On Commodity Multicore Architectures.** in Proceedings SPIE, 2009.

F. de Mesmay, S. Chellappa, F. Franchetti and M. Püschel: **Computer Generation of Efficient Software Viterbi Decoders.** Proceedings of International Conference on High-Performance Embedded Architectures and Compilers (HIPEAC), 2010.

Y. Voronenko, V. Arbatov, C. Berger, R. Peng, M. Püschel, and F. Franchetti: **Computer Generation of Platform-Adapted Physical Layer Software.** Proceedings of Software Defined Radio (SDR), 2010.

C. R. Berger, V. Arbatov, Y. Voronenko, F. Franchetti, M. Püschel: **Real-Time Software Implementation of an IEEE 802.11a Baseband Receiver on Intel Multicore.** Proceedings of International Conference on Acoustics, Speech, and Signal Processing (ICASSP), 2011.

FFT and FIR Algorithms

F. Franchetti and M. Püschel: **Generating High-Performance Pruned FFT Implementations.** Proceedings of International Conference on Acoustics, Speech, and Signal Processing (ICASSP) 09.

LC Meng, J. Johnson, F. Franchetti, Y. Voronenko, M.M. Maza and Y. Xie: **Spiral-Generated Modular FFT Algorithms.** Proc. Parallel Symbolic Computation (PASCO), pp. 169-170, 2010.

Yevgen Voronenko and Markus Püschel: Algebraic Derivation of General Radix Cooley-Tukey Algorithms for the Real Discrete Fourier Transform. Proc. International Conference on Acoustics, Speech, and Signal Processing (ICASSP), Vol. 3, 2006

Aca Gacic, Markus Püschel and José M. F. Moura: **Fast Automatic Implementations of FIR Filters.** Proc. International Conference on Acoustics, Speech, and Signal Processing (ICASSP), Vol. 2, pp. 541-544, 2003

FFTX and SpectralPACK

Carnegie Mellon

F. Franchetti, D. G. Spampinato, A. Kulkarni, D. T. Popovici, T. M. Low, M. Franusich, A. Canning, P. McCorquodale, B. Van Straalen, P. Colella: **FFTX and SpectralPack: A First Look**, IEEE International Conference on High Performance Computing, Data, and Analytics (HiPC), 2018